Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to more clearly claim Applicants invention.

Support for the amended and newly drafted claims are found in the original claims and/or the Specification. No new matter has been added. For example support for the amended claims 1, 4, 5, 8, 11, and 12 is found in the Specification at page 10 beginning at line 4:

"The present invention provides within a microelectronic fabrication a microelectronic device, and a method for fabricating the microelectronic device, wherein the microelectronic device is fabricated with **enhanced performance within a decreased microelectronic fabrication substrate area** within the microelectronic fabrication."

And at page 30 beginning at line 11:

"With respect to the enhanced performance of the field effect transistor (FET) device fabricated in accord with the present invention, **the enhanced performance is anticipated due to an increased effective channel length and/or gate electrode length** (due to corrugation of the at least one of: (1) the interface of the channel region covered by the gate electrode; and (2) the upper surface of the gate electrode) within the field effect transistor (FET) device fabricated in accord with the present invention."

And at line 10 page 11:

"As is also shown within the schematic cross-sectional diagram of Fig. 1, there is a gate electrode 14 formed over the active region 10' of the semiconductor substrate 10 and bridging to the isolation region 12, **where, as is understood by a person skilled in the art, the gate electrode 14 covers, and typically defines, a channel region within the active region 10'** of the semiconductor substrate 10."

For example support for new claims 15-20 are found in the Specification at page 15 beginning at line 3:

"Although the preferred embodiment of the present invention illustrates the present invention within the context of the silicon semiconductor substrate 20, the present invention is also applicable to forming field effect transistor (FET) devices within semiconductor substrates including but not limited to silicon semiconductor substrates and semiconductor substrates other than silicon semiconductor substrates, such semiconductor substrates other than silicon semiconductor substrates including but not limited to compound semiconductor substrates"

Claim Rejections under 35 USC 102

1. Claims 1, 2-4-6, 8, and 11-13 stand rejected under 35 USC 102(b) as being anticipated by Hayashi et al. (US 5,365,078).

Hayashi et al. disclose a device that provides for 1 and 2-dimensional conduction in a channel layer **formed on** a semiconductor substrate and an **electron supply layer formed on**

the channel layer. Hayashi et al. disclose the formation of source/drain electrodes and a gate electrode **on the electron supply layer** (see Abstract).

Hayashi et al. do not disclose Applicants disclosed and claimed invention, including a **channel region**, but disclose an electron gas FET that operates by a different principal of operation, where electron charge carriers (electron gas) are conducted through a **channel layer**, rather than a **channel region** (see col 1, lines 20-33; lines 47-51; col 2, lines 51-64).

Thus, Hayashi et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

"a gate electrode formed over the semiconductor substrate to **cover and define a channel region within the semiconductor substrate**"

or

"a pair of **source/drain regions** formed **within the semiconductor substrate** and **separated by the channel region within the semiconductor substrate**"

or

"wherein at least one of:

an interface of the channel region covered by the gate electrode; and

an upper surface of the gate electrode, is corrugated."

Rather, as stated above, in all embodiments, Hayashi et al. disclose a corrugated surface formed on an **electron supply layer** (see item 13, Figure 2) which is nowhere disclosed to cover and define a **channel region**. Rather, an electron gas is conducted in a **channel layer (see e.g., item 12, Figure 2)** extending **under** source/drain **electrodes (see items 14 and 15 Figure 2) as well as** the gate electrode. (See also, col 5, lines 36-42, col 6, lines 29-37; col 7, lines 30-35).

Hayashi et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

The Claims have been amended and new claims added to clarify Applicants' disclosed and claimed invention. A favorable reconsideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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